AMENDMENTS TO THE CLAIMS

Claims 1-30 (Cancelled)

31. (Currently Amended) A method of planarizing material formed on a processed wafer, the processed wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising:

forming a layer of first material to contact the top surface of the processed wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material to contact the top surface of the layer of first material, the layer of second material having a non-planar top surface; and

chemically-mechanically polishing the non-planar top surface of the layer of second material and the layer of first material ~~with a slurry~~ to form a planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the layer of first material having a substantially planar top surface as soon as the layer of second material is substantially all removed from the layer of first material.

32. (Previously Presented) The method of claim 31 wherein:

the planarized layer of material has a first thickness over the wafer upper level, and

the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness.

33. (Previously Presented) The method of claim 31 wherein the layer of first material is conductive and electrically connected to a device on the wafer.

34. (Previously Presented) The method of claim 33 wherein the layer of first material is polysilicon.

35. (Previously Presented) The method of claim 34 and further comprising doping the layer of polysilicon prior to forming the layer of second material.

36. (Previously Presented) The method of claim 33 wherein the layer of second material is non-conductive.

37. (Currently Amended) The method of claim 31 wherein ~~the slurry etches~~ chemically-mechanically polishing removes the layer of first material and the layer of second material at approximately a same rate.

38. (Previously Presented) The method of claim 31 and further comprising forming a layer of third material over the planarized layer of material.

39. (Previously Presented) The method of claim 38 wherein the layer of third material is a mask.

40. (Previously Presented) The method of claim 38 wherein:
the planarized layer of material includes doped polysilicon; and
the layer of third material lowers a resistance of doped polysilicon.

41. (Previously Presented) The method of claim 40 and further comprising forming a mask on the layer of third material.

42. (Currently Amended) A method of planarizing material formed on a processed wafer, the processed wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising:

conformally forming a layer of first material to contact the top surface of the processed wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material to contact and adhere to the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the layer of first material ~~with a slurry~~ to form a planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the layer of first material having a substantially planar top surface as soon as the layer of second material is substantially all removed from the layer of first material.

43. (Previously Presented) The method of claim 42 wherein:

the planarized layer of material has a first thickness over the wafer upper level, and

the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness.

44. (Previously Presented) The method of claim 42 wherein the layer of first material is conductive and electrically connected to a device on the wafer.

45. (Previously Presented) The method of claim 44 wherein the layer of first material is polysilicon.

46. (Previously Presented) The method of claim 45 and further comprising doping the layer of polysilicon prior to forming the layer of second material.

47. (Previously Presented) The method of claim 44 wherein the layer of second material is non-conductive.

48. (Currently Amended) The method of claim 42 wherein ~~the slurry etches~~ chemically-mechanically polishing removes the layer of first material and the layer of second material at approximately a same rate.

49. (Previously Presented) The method of claim 42 and further comprising forming a layer of third material over the planarized layer of material.

50. (Previously Presented) The method of claim 49 wherein the layer of third material is a mask.

51. (Previously Presented) The method of claim 49 wherein:
the planarized layer of material includes doped polysilicon; and
the layer of third material lowers a resistance of doped polysilicon.

52. (Previously Presented) The method of claim 51 and further comprising forming a mask on the layer of third material.